IN THE CLAIMS:

Please amend the claims as follows:

Claim 1 (Currently Amended): A memory providing apparatus for an image data interpolation in an image processing system having an image sensor outputting line image data from a sensed image, comprising:

a readable and writable single memory;

a buffer register having a prior data area storing first line image data, which has been stored in the memory, in a unit of 2 m bits, and having a present data area storing second line image data, which is inputted in a unit of m bits, in a unit of the 2 m bits; and

a memory controller providing the memory with a chip enable signal, a write enable signal, and an address indicating locations of the first and second line image data stored in the buffer register, reading and writing the first and second line image data from and on the memory, and outputting the first and second line image data and a third line image data, which is inputted from the image sensor,

wherein the memory comprises a 4 m bits memory cell having upper and lower areas storing in a memory cell unit of 2 m bits data, respectively, which are readable and writable by the memory controller, and

wherein the memory controller controls the chip enable signal and the write enable signal to be enabled and disabled, respectively, and reads the first line image data from the memory

when the chip enable signal and the write enable signal are enabled and disabled, respectively, to store the first line image data in the prior data area of the buffer register, and the memory controller controls the chip enable signal and the write enable signal to be enabled, and stores the first and second line image data, which have been stored in the buffer register, in the memory in a unit of the memory cell unit.

Claim 2 (Original): The apparatus of claim 1, further comprising: an image signal processor performing an image data interpolation when receiving the first, second, and third line image data from the memory controller.

Claim 3-4 (Cancelled).

Claim 5 (Currently Amended): The apparatus of claim [[3]] 1, further comprising:

an image signal processor performing a 3x3 line interpolation using the first, second, and third line image data; and

first, second, and third data transmission lines through which the first, second, and third line image data are outputted from the memory controller, respectively,

wherein the memory controller reads the first and second line image data stored in the memory, transmits the first and second line image data through the first and second data transmission lines, and transmits the third line image data, which is inputted from the image sensor, through the third data transmission line according to [[the]] a same clock.

Claim 6 (Original): The apparatus of claim 1, wherein the memory controller comprises: three data transmission lines through which the first, second, and third line image data are outputted from the memory controller.

Claim 7 (Currently Amended): ~~The~~ A memory providing apparatus ~~of claim 1~~ for an image data interpolation in an image processing system having an image sensor outputting line image data from a sensed image, ~~further~~ comprising:

a readable and writable single memory;

a buffer register having a prior data area storing first line image data, which has been stored in the memory, in a unit of 2 m bits, and having a present data area storing second line image data, which is inputted in a unit of m bits, in a unit of the 2 m bits;

a memory controller providing the memory with a chip enable signal, a write enable signal, and an address indicating locations of the first and second line image data stored in the buffer register, reading and writing the first and second line image data from and on the memory, and outputting the first and second line image data and a third line image data, which is inputted from the image sensor; and

an image signal processor performing a 3x3 line interpolation using the first, second, and third line image data; and

first, second, and third data transmission lines through which the first, second, and third line image data are outputted from the memory controller, respectively,

wherein the memory controller reads the first and second line image data stored in the memory, transmits the first and second line image data through the first and second data transmission lines, and transmits the third line image data, which is inputted from the image sensor, through the third data transmission line according to [[the]] a same clock.

Claim 8 (Original): The apparatus of claim 1, wherein the line image data comprises: a Bayer pattern.

Claim 9 (Original): The apparatus of claim 1 wherein the image sensor comprises: one of a charge coupled device image sensor and a complementary metal oxide semiconductor.

Claim 10 (Currently Amended): A method of providing line data for interpolation in an image processing system, the method comprising:

storing first line image data outputted from an image sensor in a unit of m bits in a present data area of a buffer register in a unit of 2 m bits;

storing the first line image data of the present data area of the buffer register in a memory in the unit of the 2 m bits;

refreshing the buffer register;

reading the first line image data from the memory in the unit of the 2 m bits to store the read first line image data in a prior data area of the buffer register, and storing second line image data outputted from the image sensor in the unit of the m bits in the present data area of the

buffer register in the unit of the 2 m bits;

storing the first line image data and the second line image data stored in the prior data area and the present data area of the buffer register, respectively, in the memory in a unit of 4 m bits; and

transmitting the first and second line image data stored in the memory and third line image data outputted from the image sensor to an image signal processor according to [[the]] a same clock signal.

Claim 11 (Original): The method of claim 10, wherein the transmitting of the first, second, and third line image data comprises: reading the first line image data stored in the memory using a memory controller-connected to the memory; reading the second line image data stored in the memory using the memory controller; and outputting the third line image data inputted from the image sensor and the first and second line image sensor to the image signal processor through respective data transmission lines.

Claim 12 (Original): The method of claim 10, wherein the transmitting of the first, second, and third line image data comprises: causing first and second data transmission lines to be connected between the memory and the image signal processor, and causing a third data transmission line to be connected between the image sensor and the image signal processor; and outputting the first line image data through the first data transmission line, the second line image data through the second data transmission line, and the third line image data through the third

data transmission line according to the same clock signal.

Claim 13 (Original): The method of claim 10, wherein the memory has a capacity able to store two line image data.

Claim 14 (Original): The method of claim 10, wherein each of the first, second, and third line image data comprises a series of pixel data.

Claim 15 (New): The apparatus of claim 7, wherein the memory comprises a 4 m bits memory cell having upper and lower areas storing in a memory cell unit of 2 m bits data, respectively, which are readable and writable by the memory controller

Claim 16 (New): The apparatus of claim 7, wherein the line image data comprises a Bayer pattern.

Claim 17 (New): The apparatus of claim 7, wherein the image sensor comprises one of a charge coupled device image sensor and a complementary metal oxide semiconductor.